wiring layer 8 is formed by laminating polyimide and aluminum layers on the semiconductor chip 2. As further seen in Figure 3, the second semiconductor chip 3 is mounted on the wiring layer by an adhesive material 4 and the wiring layer 8 is provided on the first semiconductor chip 2 without using an adhesive material.

The Official Action offers Figure 7 of TAKIAR et al. as teaching a wiring layer 138 between first and second semiconductor chips 136, 140 and that the second semiconductor chip 140 is mounted on the wiring layer 138 by an adhesive material 88. The Official Action states that TAKIAR et al. teach a wiring layer comprising a substrate material which is defined as including a conductor such as copper or aluminum and a dielectric such as a polyimide. This assertion is not supported by the reference.

Specifically, column 4, lines 50-60 of TAKIAR et al., for example, disclose that a substrate material may be, but is not limited to, ceramic, metal, silicon or a plastic circuit board material. The metal can include aluminum and copper. TAKIAR et al. at column 4, line 67 through column 5, line 2 teach that the plastic circuit board (PCB) material or dielectric can be either polyimide or SiO_2, both of which are standard dielectrics in IC fabrication. Accordingly, TAKIAR et al. teach either a metal such as aluminum or a dielectric plastic circuit board material such as polyimide but do not teach or suggest that

the substrate material includes both the metal and the dielectric as indicated in the Official Action.

The Official Action further states that TAKIAR et al. fail to show that the wiring layer is provided on the first semiconductor chip without using an adhesive material. This shortcoming is attempted to be overcome by combining TAKIAR et al. with SHINOHARA.

SHINOHARA teaches forming a film on a semiconductor device using a spin coating method. Column 1, lines 11-24 of SHINOHARA teach that a polyimide layer is formed using a spin coating method between a mold resin and a passivation film to reduce stress generated between the mold resin and the passivation film due to variations in temperature. Adding an extra layer of polyimide between the mold resin and the passivation film would increase the size of the semiconductor chip package, not reduce the size of the semiconductor chip package as noted in the Official Action. Therefore, the motivation provided in the Official Action is not supported by the reference.

MPEP §2143.01 states that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

In each of the figures of TAKIAR et al., especially Figure 7, TAKIAR et al. initially start with a substrate 142, then an adhesive layer, then the first chip 136, then an adhesive layer and then the wiring layer 138. These layers are successively formed smaller than the previous layer so that electrical contacts can be mounted on the top surface of each of the layers 136, 138 to connect these layers with the substrate 142. Accordingly, applying the method of SHINOHARA would entail rotating both the substrate and the chip. The resultant polyimide layer would cover the entirety of the first chip 136. Time-consuming and costly additional steps would be required to remove the excess polyimide layer from the chip so that the contact could be formed on the chip. Therefore, there is no desirability of using such a process on a multi-chip module as taught by TAKIAR et al.

In addition, as noted above, the polyimide film in SHINOHARA is for relieving stress between a mold resin and a passivation film. SHINOHARA does not teach or suggest a copper foil layer within the polyimide layer. TAKIAR et al. at column 6, lines 36-42, for example, teach a contact strip 68 on the substrate as seen in Figure 2. The combination of references do not teach or suggest a wiring layer which includes a polyimide tape having a copper foil layer therein as recited in claim 7 of the present application.

For the reasons set forth above, one of ordinary skill in the art would not be motivated to combine SHINOHARA with TAKIAR et al. to render obvious claim 7 of the present application. In addition, the resultant combination does not teach all of the claim limitations as required for a *prima facie* case of obviousness.

Claim 8 depends from claim 7 and further defines the invention and is also believed patentable over the combination of references.

Claim 12 also recites a wiring layer between first and second semiconductor chips, the wiring layer including a conductor within the wiring layer, wherein the second semiconductor chip is mounted on the wiring layer by an adhesive material and the wiring layer is provided on the first semiconductor chip without using an adhesive material. The comments above regarding claim 7 are equally applicable to claim 12. Claims 14 and 15 depend from claim 12 and further define the invention and are also believed patentable over the cited prior art.

Claim 17 recites a wiring layer between first and second semiconductor chips, the wiring layer including a conductor traversing the wiring layer, wherein the second semiconductor chip is mounted on the wiring layer by an adhesive material and the wiring layer is provided on the first semiconductor chip without using an adhesive material. The

comments above regarding claim 7 are equally applicable to claim 17.

Claims 9, 13 and 19 are rejected as unpatentable over TAKIAR et al. in view of SHINOHARA and further in view of BEILSTEIN, JR. et al. 5,567,654. This rejection is respectfully traversed.

BEILSTEIN, JR. et al. is cited for the teaching of a connection wire for connecting one bonding pad on the wiring layer to another bonding pad on the wiring layer. BEILSTEIN, JR. et al. do not teach or suggest what is recited in claims 7, 12, and 17. As noted above, TAKIAR et al. in view of SHINOHARA do not teach or suggest what is recited in claims 7, 12 and 17. Since claims 9, 13 and 19 depend from claim 7, 12, and 17, respectively, and further define the invention, the combination of references would not render obvious claims 9, 13 and 19.

Claims 10, 11, 16, 18 and 20 are rejected as unpatentable over TAKIAR et al. in view of SHINOHARA and further in view of TOKUDA et al. 5,870,289. This rejection is respectfully traversed.

TOKUDA et al. is cited for the teaching of a direct through-hole connection through a wiring layer which connects to a bonding pad of a chip. TOKUDA et al. do not teach or suggest what is recited in claims 7, 12 and 17. As noted above, TAKIAR et al. in view of SHINOHARA do not teach or suggest what is recited in claims 7, 12 and 17. Since claims 10, 11, 16 and 18

depend from claims 7, 12 and 17, respectively, and further define the invention, the combination of references would not render obvious claims 10, 11, 16 and 18.

Claim 20 recites a wiring layer between first and second semiconductor chips, the wiring layer including a polyimide tape having a copper foil layer therein.

As noted above, TAKIAR et al. at column 4, line 50 through column 5, line 5 disclose a substrate material is ceramic, metal, silicon or a plastic circuit board (PCB) material. TAKIAR et al. do not teach or suggest combinations of these materials, specifically not a polyimide tape having a copper foil layer therein as recited in claim 20 of the present application. SHINOHARA is cited for the teaching of a polyimide coating and does not teach or suggest a wiring layer including a polyimide tape having a copper foil layer therein.

TOKUDA et al. in Figure 1 and as disclosed on column 10, lines 52-57, for example, teach a wiring substrate 20 made of a polyimide film. Copper wires 21 are etched or plated onto the polyimide substrate 20. The two-layer connection of TOKUDA et al. with an exposed wiring is neither a polyimide tape with a copper foil layer interposed therein as disclosed on page 5, lines 2-3 of the present application, nor a wiring layer including a polyimide tape having a copper foil layer therein as recited in claim 20 of the present application. The above-noted feature is missing from each of the references, is absent from

the combination and thus is not obvious to one having ordinary skill in the art. Accordingly, claim 20 is also believed patentable over the cited prior art.

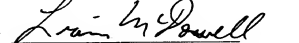
Claim 21 is rejected as unpatentable over TAKIAR et al. in view of SHINOHARA and further in view of TOKUDA et al. and BEILSTEIN, JR. et al. This rejection is respectfully traversed.

BEILSTEIN, JR. et al. is cited for the teaching of a connection wire for connecting one bonding pad on the wiring layer to another bonding pad on the wiring layer. BEILSTEIN, JR. et al. do not disclose or suggest what is recited in claim 20. As noted above, neither TAKIAR et al. nor SHINOHARA nor TOKUDA et al. teach or suggest what is recited in claim 20. Since claim 21 depends from claim 20 and further defines the invention, the combination of references would not render obvious claim 21.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

Respectfully submitted,

YOUNG & THOMPSON

By 

Liam McDowell
Attorney for Applicant
Registration No. 44,231
745 South 23rd Street
Arlington, VA 22202
Telephone: 703/521-2297

January 24, 2003